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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,439	01/31/2006	Eckhard Wolfgang	1454.1671	3860

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,439	WOLFGANG ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 11-21, 23 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hase et al. (WO 2003/030247; cited by Applicant)** in view of **Chu et al. (US 6,365,498; cited by Applicant)**. Note that the WO 2003/030247 reference is a publication of international application PCT/DE02/03615, and that the U.S. application 10/491137 is a national stage entry of the international application. Therefore, the U.S. 2005/0032347 document, which is a publication of the U.S. application 10/491137, will be used as an English translation for the WO 2003/030247 reference.

With respect to **claims 11 and 24, Hase** teaches a circuit device provided on a substrate **(10-12, Fig. 2 of US 2005/0032347)** and comprising:

a single active semiconductor component **(2, Fig. 2; ¶ [0056])** arranged on a top surface of the substrate **(10-12)** and having an outer electrical contact surface **(¶ [0068]; top surface of chip 2, Fig. 2)**;

at least one electrical connection line **(4, Fig. 2; ¶ [0070])** on the substrate **(10-12)** to contact with the outer electrical contact surface of the semiconductor component **(¶ [0070])**,

wherein the electrical connection line **(4, Fig. 2)** contacts the outer electrical contact surface at an electrical contact, such the electrical contact faces away from the substrate **(¶ [0070]-[0071])**; and

a layer of laminated electrically insulating film **(3, Fig. 2)** is laminated onto a least two surfaces of the semiconductor component **(2, Fig. 2; ¶ [0063])** and the substrate **(10-12)** in such a way that the electrical contact is exposed **(Fig. 2; ¶ [0067])**.

Thus, **Hase** teaches all the limitations of the claim with the exception of explicitly disclosing wherein the electrical connection line is part of at least one discrete passive electrical component arranged on the substrate.

However, **Chu** teaches a circuit device on a substrate **(22, Fig. 3)** wherein an electrical connection line **(40, Fig. 3)** is part of at least one discrete passive component **(48, Fig. 3; col. 6, lns. 3-18)** arranged on the substrate **(22)**. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the teaching of Chu into the device of Hase, thereby forming a passive electrical component using a part of an electrical connection line, for the purpose of providing integrated circuit devices with both active and passive elements, while reducing manufacturing costs by integrating methods for I/O redistribution and passive components fabrication **(Chu: col. 4, lns. 58-60)**.

With respect to **claim 12,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is a capacitor **(48, Fig. 3; col. 6: lns. 5-21)** and the electrical connection line **(40)** is an electrode of the capacitor **(48)**.

With respect to **claim 13,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is a coil **(36, Fig. 2E)**, and the electrical connection line **(30; col. 5: lns. 57-67)** is a winding of the coil **(col. 4: lns. 45-48)**.

With respect to **claim 14,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is an electrical resistor **(36, 38, Figs. 2C and 2D)**, and the electrical connection line **(30)** is a wire resistor **(col. 5: lns. 57-67)**.

With respect to **claim 15,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is a part of a sensor of a physical variable **(the electrical wire resistors 36 and 38, formed from connection line 30 can act as temperature sensors)**.

With respect to **claim 16 and 17,** which is dependent on claim 11, **Hase** teaches wherein the semiconductor component is a power semiconductor component **(¶ [0058])**, and regarding the limitations of MOSFETs, IGBTs and bipolar transistors, note that such active semiconductor components are well known and conventional in the art.

With respect to **claim 18,** which is dependent on claim 14, **Chu** teaches wherein the discrete passive electrical component is a part of a sensor of a physical variable **(the electrical wire resistors 36 and 38, formed from connection line 30, can act as temperature sensors)**.

With respect to **claims 19 and 20**, which is dependent on claim 18, **Hase** teaches wherein the semiconductor component is a power semiconductor component **(¶ [0058])**, and regarding the limitations of MOSFETs, IGBTs and bipolar transistors, note that such active semiconductor components are well known and conventional in the art.

With respect to claim 21, **Hase** teaches a method for producing a circuit device **(Fig. 2 of US 2005/0032347)**, comprising:

producing a single active semiconductor component **(2, Fig. 2; ¶ [0056])** on a top surface of the substrate **(10-12, Fig. 2)**, the semiconductor component having an outer electrical contact surface **(¶ [0068]; top surface of chip 2, Fig. 2)** facing away from the substrate; and

producing an electrical connection line **(4, Fig. 2; ¶ [0070])** that o contact with the outer electrical contact surface of the semiconductor component **(¶ [0070])**,

wherein the electrical connection line **(4, Fig. 2)** contacts the outer electrical contact surface at an electrical contact, such the electrical contact faces away from the substrate **(¶ [0070]-[0071])**; and

laminating a layer of electrically insulating film **(3, Fig. 2)** onto the semiconductor component **(2, Fig. 2; ¶ [0063])** and the substrate **(10-12)** in such a way that the electrical contact is exposed **(Fig. 2; ¶ [0067])**.

Thus, **Hase** teaches all the limitations of the claim with the exception of explicitly disclosing wherein the electrical connection line is part of one discrete passive electrical component arranged on the substrate.

However, **Chu** teaches a circuit device on a substrate **(22, Fig. 3)** wherein an electrical connection line **(40, Fig. 3)** is part of one discrete passive component **(48, Fig. 3; col. 6, lns. 3-18)** arranged on the substrate **(22)**. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the teaching of Chu into the device of Hase, thereby forming a passive electrical component

using a part of an electrical connection line, for the purpose of providing integrated circuit devices with both active and passive elements, while reducing manufacturing costs by integrating methods for I/O redistribution and passive components fabrication **(Chu: col. 4, lns. 58-60)**.

With respect to **claim 23,** which is dependent on claim 21, **Hase** teaches wherein the layer of electrically insulating film **(3, Fig. 2)** is first applied, and then the electrical contact is exposed by opening a window **(31, Fig. 2)** in the electrically insulating material **(¶ [0063]-[0067])**.

Response to Arguments

2. Applicant's arguments filed July 18, 2008, have been considered but are moot in view of new grounds of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814